International Journal Of Advanced Research In Engineering Technology & Sciences
ISSN: 2394-2819
Email: editor@ijarets.org March- 2015 Volume 2, Issue-3 www.ijarets.org

Study and Implementation of CSI-2 Receiver and Lane Merging

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ABSTRACT
In this paper, we present, multi-lane Mobile Industry Processor Interface (MIPI) Camera Serial Interface (CSI) receiver which is suitable for high-resolution camera and high-density (HD) video applications. The presented receiver is designed to achieve parallel processing so that it reduces dynamic power consumption for multi-lane configuration. In order to facilitate parallel processing, we purpose two techniques for multi-lane receiver. The presented designs receives data at the maximum rate of 4Gb/s .

Key Words— MIPI, Multi-lane system, Camera application, CSI-2.

I. INTRODUCTION

Demands for increasingly higher resolution and density are pushing the bandwidth capacity in mobile camera applications. Parallel interfaces which are typically employed in conventional camera systems are difficult to meet the wide bandwidth requirements because they need many interconnects and consume relatively large amounts of power. To overcome aforementioned barriers, Mobile Industry Processor Interface (MIPI) alliance was established to define and promote open standards for hardware and software interfaces between processors and peripherals in mobile systems. Especially, MIPI Camera Serial Interface (CSI) standard has drawn remarkable attention and has been rapidly replacing conventional parallel interfaces in mobile camera systems. In the CSI standard, the two types of lane configurations (single lane / multi-lane) are defined. Among them, multi-lane structure becomes more popular in high-resolution camera and High-Density (HD) video applications than single lane configuration because of its higher bandwidth nature. However, due to the byte-oriented feature of the CSI standard, the multi-lane receiver requires parallel processing techniques to process multiple packet bytes within a single transmission cycle, otherwise it needs to employ faster clock rate which results in high dynamic power consumption. For instance, byte (8 bits) rate that needs to be processed becomes125MHz when transmission bit rate is 1Gb/s in a single lane structure. Meanwhile, in case of a four-lane structure, byte rate is four times higher than single lane structure, thus the system should process a packet byte at a rate of 500MHz (125MHz ×4) for the same bit rate (1Gb/s) per data lane. In this paper, we propose a Lane merger unit and a Cascade CRC unit to facilitate parallel processing in receiving for a multi-lane MIPI CSI receiver. The proposed Lane merger unit packs multiple packet bytes into a single data word from multiple data lanes regardless of the lane configurations, thus it can hold a single clock rate and provide scalability from one to multiple data lanes. Also, the proposed Cascade-CRC unit calculates a checksum over multiple payload bytes within a single clock cycle. The presented receiver achieves parallel processing using the proposed techniques so that reduces dynamic power consumption where it is configured to multiple data lanes barriers

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consumption. For instance, byte (8 bits) rate that needs to be processed becomes125MHz when transmission bit rate is 1Gb/s in a single lane structure. Meanwhile, in case of a four-lane structure, byte rate is four times higher than single lane structure, thus the system should process a packet byte at a rate of 500MHz (125MHz ×4) for the same bit rate (1Gb/s) per data lane.

II. MIPI CSI STANDARD OVERVIEW

In this section, we will briefly overview the MIPI CSI standard to describe only the presented receiver. MIPI CSI is realized with two separate specifications. One is physical layer specification, referred as D-PHY specification, that specifies two types of signalling, data transmission, and electrical characteristics and another is protocol layer specification, referred as CSI-2 specification, that specifies control interfaces and packet transmission protocol that defines how arbitrary data are to be transported from the transmitter to the receiver

A.D-PHY Specification

D-PHY specification specifies a source synchronous, high speed, low-power, and physical layer communication, especially suited for mobile camera applications. It uses two wires per data lane plus two wires for the clock lane, thus requires four wires for the minimum connection. The clock signal is unidirectional, originating from the transmitter and terminating at the receiver. The data signal can either be unidirectional or bi-directional. The link includes a High Speed (HS) signalling mode for fast-data traffic and a Low Power (LP) signalling mode for control purpose.

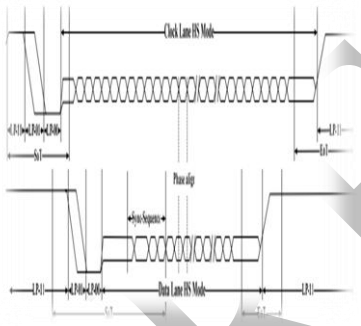

Fig.1.High-Speed Data Transmission In Bursts

HS data communication appears in bursts with an arbitrary number of packet bytes. In HS mode, each lane is terminated on both sides and driven by a low-voltage swing, differential signal. In LP mode, all wires are operated single-ended and non-terminated.

Fig. 1 shows the sequence of events during the transmission of a data burst. HS data transmission occurs in bursts and it starts from, and ends with, a Stop-state (LP-11). More details, the clock lane leaves Stop-state and prepares for HS mode by means of a Start-of-Transmission (SoT) procedure: LP-11 →LP-01 → LP-00. The clock lane shall be in HS mode before the data lane commences a data burst, providing Double Data Rate (DDR) clock signal that is respect to the toggling bit sequence of the data. The clock lane shall remain in the HS mode until the data lane completes a data burst then returns to Stop-state by means of an End-of-Transmission (EoT) procedure: LP-00 → LP-11.

The data lane also leaves Stop-state and prepares for HS mode by means of a SoT procedure. In HS mode, valid bits are transmitted just after transmitting the Sync-Sequence: 00011101. At the end of a data burst, the data lane returns to Stop-state by means of an EoT procedure. During the intermediate time between transmission bursts, the data lane shall remain in Stop-state.

B.CSI-2 Specification

CSI-2 specification. Specifies control interfaces and packet transmission protocol to inform how arbitrary data are to be transported from the transmitter to the receiver. It is a byte oriented, packet based protocol that

transports arbitrary data using Short packet and Long packet. A Short packet and a Long packet are used for low-level protocol communication and each packet is distinguished by the data type field in the packet header. Long packet consists of three elements: a 32-bit Packet Header (PH), payload data with arbitrary number of 8-bit data words, and a 16-bit Packet Footer (PF). In the Long packet, the PH is further composed of three elements: an 8-bit data Identifier (DI), a 16-bit Word Count (WC) field, and an 8-bit Error Correction Code (ECC). In the PH, the DI contains 2-bit virtual channel identifier for the data and 6-bit data type information. The data type denotes the format/content of the payload data. The WC field defines the number of 8-bit data words of the payload data between the end of the PH and the start of the PF. The ECC is used for correcting single-bit errors and detecting double-bit errors in the PH. The PF has one element, a 16-bit checksum.
Short packet consists of only one element: a PH. In the PH, the data type is used for the frame/line synchronization codes and the WC field is replaced to the frame/line number.

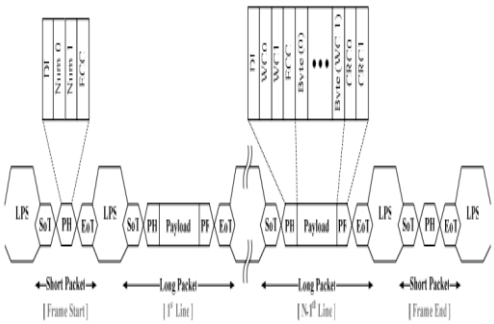

Fig.2. Packet Transmission Protocol for Camera Applications

III. CSI-2 LAYER DEFINITIONS

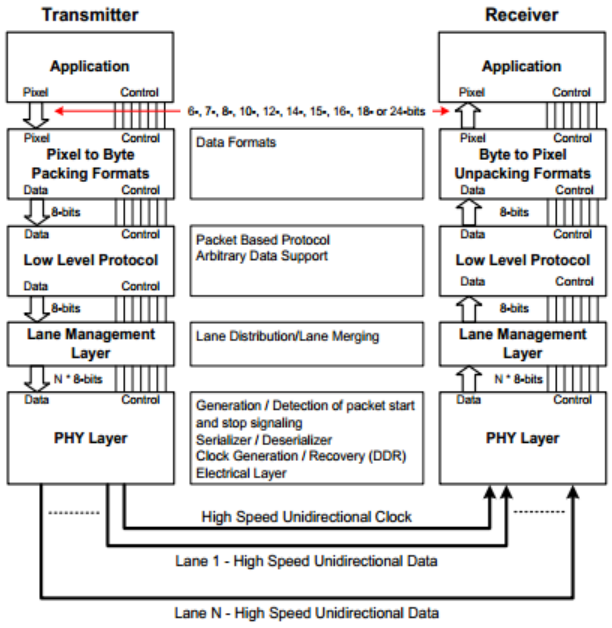

Fig.3.CSI-2 Layer Definition

a).PHY Layer:-The PHY Layer specifies the transmission medium (electrical conductors), the input/output circuitry and the clocking mechanism that captures "ones" and "zeroes" from the serial bit stream. This part of the specification documents the characteristics of the transmission medium, electrical parameters for signalling and the timing relationship between clock and data Lanes. The mechanism for signalling Start of

Transmission (SoT) and End of Transmission (EoT) is specified as well as other "out of band" information that can be conveyed between transmitting and receiving PHYs. Bit-level and byte-level synchronization mechanisms are included as part of the PHY.

b).Protocol Layer:-The Protocol layer is composed of several layers, each with distinct responsibilities. The CSI-2 protocol enables multiple data streams using a single interface on the host processor. The Protocol layer specifies how multiple data streams may be tagged and interleaved so each data stream can be properly reconstructed.

c).Pixel/Byte Packing/Unpacking Layer:- The CSI-2 supports image applications with varying pixel formats from six to twenty-four bits per pixels. In the transmitter this layer packs pixels from the Application layer into bytes before sending the data to the Low Level Protocol layer. In the receiver this layer unpacks bytes from the Low Level Protocol layer into pixels before sending the data to the Application layer. Eight bits per pixel data is transferred unchanged by this layer.

d).Low Level Protocol:-The Low Level Protocol (LLP) includes the means of establishing bit- level and byte-level synchronization for serial data transferred between SoT (Start of Transmission) and EoT (End of Transmission) events and for passing data to the next layer. The minimum data granularity of the LLP is one byte. The LLP also includes assignment of bit-value interpretation within the byte, i.e. the "Endian" assignment.

e).Lane Management:-CSI-2 is Lane-scalable for increased performance. The number of data Lanes may be one, two, three or four depending on the bandwidth requirements of the application. The transmitting side of the interface distributes ("distributor" function) the outgoing data stream to one or more Lanes. On the receiving side, the interface collects bytes from the Lanes and merges ("merger" function) those together into a recombined data stream that restores the original stream sequence. Data within the Protocol layer is organized as packets. The transmitting side of the interface appends header and optional error-checking information on to data to be transmitted at the Low Level Protocol layer. On the receiving side, the header is stripped off at the Low Level Protocol layer and interpreted by corresponding logic in the receiver. Error-checking information may be used to test the integrity of incoming data.

f).Application Layer:-This layer describes higher-level encoding and interpretation of data contained in the data stream. The CSI-2 specification describes the mapping of pixel values to bytes.

IV. MULTIl-LANE CSI-2 RECEIVER

Physical layer communication is established with an independent unit of physical-layer logic and transmission circuitry for each lane. Thus, a multi-lane structure links one clock lane and two or more data lanes between the transmitter and the receiver. In this work, we designed a four-data lane receiver, thus it has one D-PHY module for the clock lane and four D-PHY modules for the data lanes inside. The D-PHY module for the data lane consists of a HS mode buffer, a LP mode buffer, a De-serializer, a Sync-Finder, and control logics. The D-PHY module for the clock lane has the same components inside, except a De-serialzer and a Sync-Finder. The D-PHY module for the clock lane recovers DDR clock in HS mode then outputs In/Quadrature-phase clock signals. The D-PHY module for the data lanes recovers the serial data signal then de-serializes it, using the In/Quadrature-phase clocks, to 8-bit data word (packet byte) in HS mode, generating a byte-clock which is respected to the byte sequence.

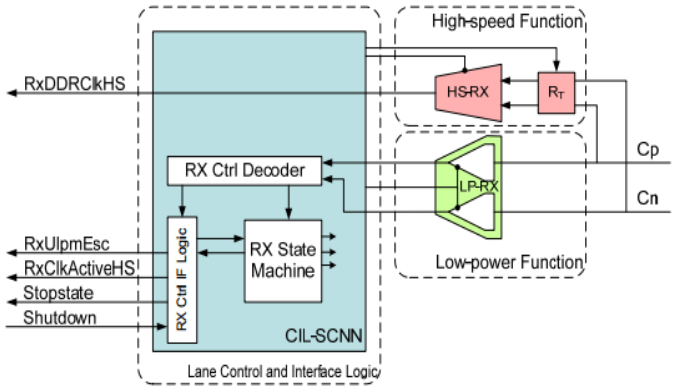

Fig.4.D-PHY Module for Clock Lane

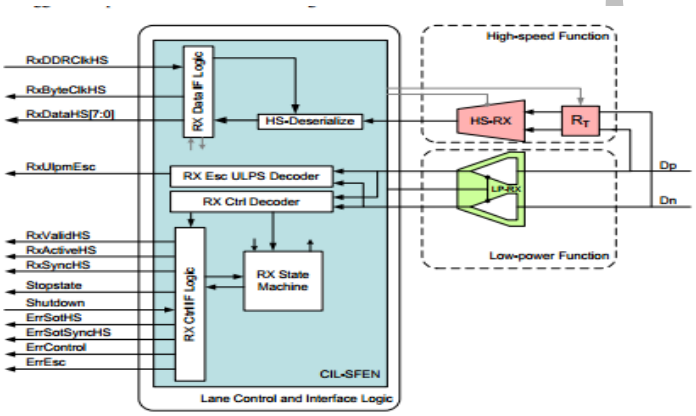

Fig.5.D-PHY Module For Data Lane

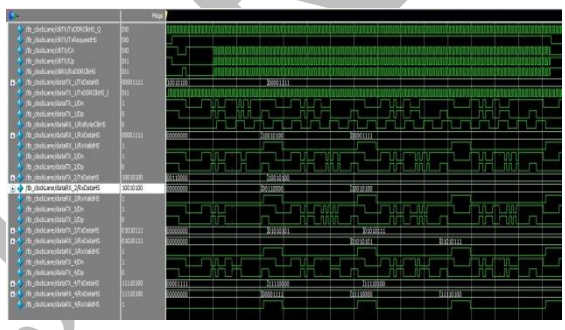

Fig.6.D-PHY: Four Data Lane + One Clock Lane

V. PROPOSED LANE MERGER UNIT

In multi-lane structures, packet bytes are distributed to each data lane. The transmitter distributes a sequence of packet bytes across N data lanes, where each data lane is an independent unit of physical layer logic and transmission circuitry. Thus, the receiver collects incoming packet bytes from N data lanes and consolidates them into complete packets to pass into the packet decompose stage. The proposed Lane merger unit sequentially reorders incoming packet bytes from four data lanes and packs it into a four-byte word to hold a single clock rate regardless of the data lane configurations and to provide scalability from one to four data lanes. If the receiver is configured to single data lane, it selects a data lane and packs an incoming packet byte into a four-byte word then outputs it at the fourth clock cycle. If the receiver is configured to two data lanes, it selects two data lanes and packs two incoming packet bytes into a four-byte word then outputs it at the second clock cycle. Lastly, if the receiver is configured to four data lanes, it reorders four incoming packet bytes sequentially then packs it into a fourbyte word then outputs it per clock cycle.

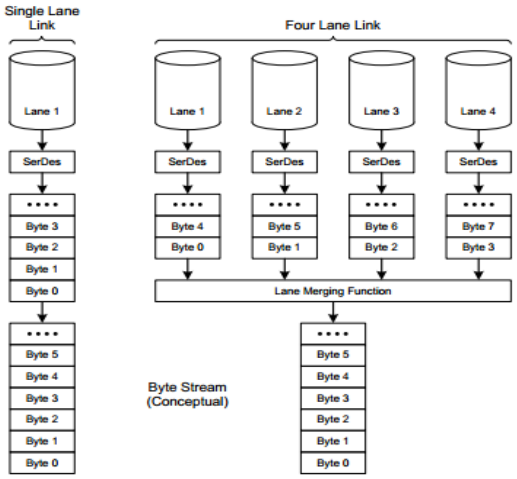

Fig.7.Lane Merging Function

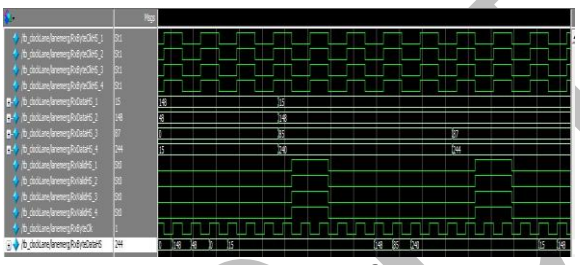

Fig.8.Lane merging function

VI. LOW LEVEL PROTOCOL

The LLP is a byte orientated, packet based protocol that supports the transport of arbitrary data using Short and Long packet formats. There are some following features of low level protocol(LLP) which are describing below:

a). Transport of arbitrary data (Payload independent)
b).8-bit word size
c). Support for up to four interleaved virtual channels on the same link.
d). Special packets for frame start, frame end, line start and line end information.
e). Descriptor for the type, pixel depth and format of the Application Specific Payload data.
f).16-bit Checksum Code for error detection.

Long packet and Short packet structures are explained for LLP communication. For each packet structure exit from the low power state followed by the Start of Transmission (SoT) sequence indicates the start of the packet. The End of Transmission (EoT) sequence followed by the low power state indicates the end of the packet. Long packet provide three elements: a 32 bit Packet header (PH), Payload data with arbitrary number of 8-bit data words and a 16-bit Packet footer(PF).PH is further composed of three elements:8-bit data identifier(DI).a 16-bit word count(WC) field, and an 8-bit Error correction code(ECC).In the PH the DI contains 2-bit virtual channel identifier for the data and 6-bit data type payload data. The WC field defines the number of 8-bit data words of the payload data between the end of the PH and the start of PF. The ECC is used for correcting single-bit errors and detecting double-bit errors in the PH. The PF has one element a 16-bit checksum.

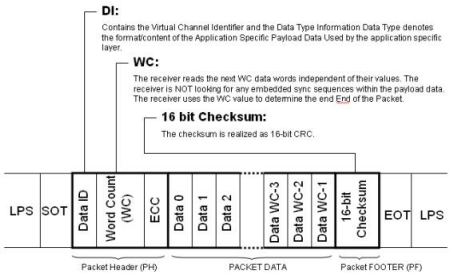

Fig.9.Long packet structure

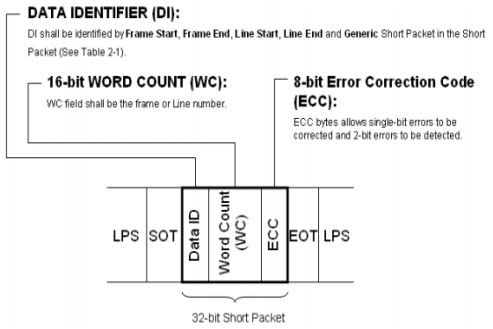

Fig.10.Short packet structure

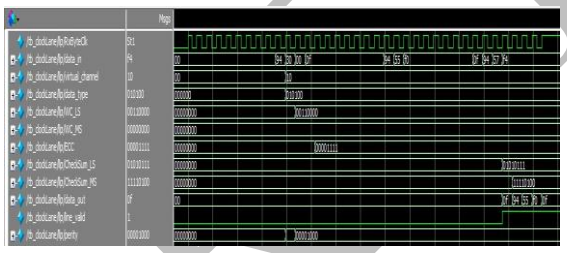

Fig.11.Low Level Protocol

VII. PROPOSED CASECADE-CRC UNIT

A checksum is calculated over each data packet to detect possible errors in transmission. The checksum is realized as 16-bit CRC and the generator polynomial is x^16+x^12+x^5+x^0 The 16-bit checksum sequence is transmitted as part of the Packet Footer. The CRC shall be 0xFFFF when the Word Count is zero. At the beginning of each packet, the CRC shift register is initialized to 0xFFFF. After all payload data has passed through the CRC circuitry, the CRC circuitry contains the checksum. Figure shows the final contents of the 16-bit checksum shift register. In the transmission, the checksum is then sent over CSI-2 bus to the receiver to verify that no errors have occurred.

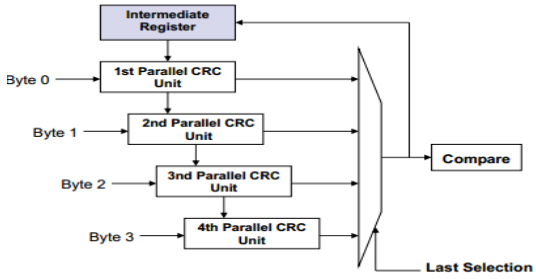

Fig.12.Proposed Cascade-CRC Unit

Above figure showing the first parallel CRC calculation unit calculates a checksum over r=the first payload byte and passes it to second stage. Then second CRC unit calculates a checksum over the second payload byte with checksum which was already calculated in the previous stage. This serious of calculation continouse to the last stage then checksum of the last stage is latched on the intermediate register. The latched checksum is to be used for calculating a checksum over next following payload byte. In this way we can proposed a CRC unit calculates a checksum over four payload bytes per clock cycle and can be easily further extended.

VIII .DESCRIPTION OF CSI-2 RECEIVER

Fig shows the multi-lane MIPI CSI receiver. It consists of one D-PHY module for clock lane, four D-PHY module for data lanes, Cascade-CRC unit, ECC generator, PH decoder, Buffer manager, PHY controller. The CSI-2 implementation example supposes that the interface comprises of D-PHY unidirectional Clock and Data. For this implementation example a layered structure is included the following parts:

a).D-PHY implementation
b). Multi Lane Merger
c).LLP

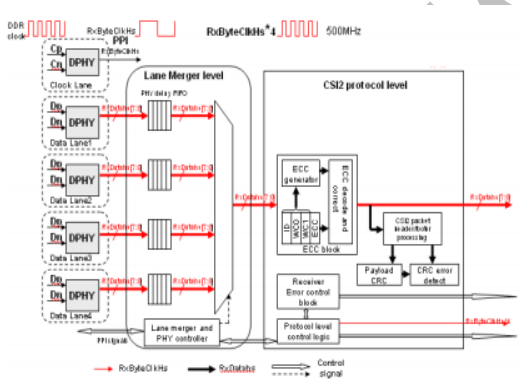

Fig.13.CSI-2 Receiver Block Diagram

VIII. RESULT AND DISCUSSION

Its result showing successfully studied and implemented CSI receiver. Its result showing how the CSI receiver formed by using layer architecture.

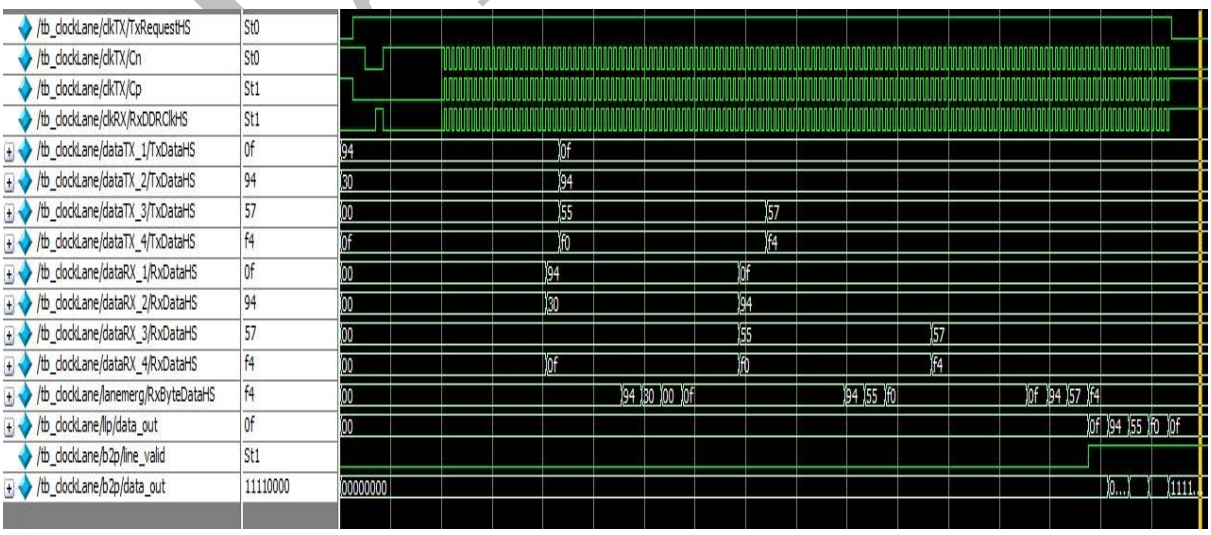

Fig.14.CSI Receiver

IX. CONCLUSION

In this paper we present a multi-lane MIPI CSI receiver which is suitable for high resolution camera and HD video applications. The presented multi-lane receiver designed to achieve parallel processing so that reduces dynamic power consumption when it is configured to multiple data lanes. We described how the proposed lane merger unit and cascades-CRC unit facilitate parallel processing in receiving and how the proposed techniques can be further extended. Consequently, we expected that the proposed technique can be easily adopted for a multi-lane MIPI CSI receiver and implementation results prove the efficiency.

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